

NCN5150

Wired M-BUS Slave Transceiver

Description

The NCN5150 is a single-chip integrated slave transceiver for use in two-wire Meter Bus (M-BUS) slave devices and repeaters. The transceiver provides all of the functions needed to satisfy the European Standards EN 13757-2 and EN 1434-3 describing the physical layer requirements for M-BUS. It includes a programmable power level of up to 2 (SOIC version) or 6 (NQFP version) unit loads, which are available for use in external circuits through a 3.3 V LDO regulator.

The NCN5150 can provide communication up to the maximum M-BUS communication speed of 38,400 baud (half-duplex).

Features

- Single-chip MBUS Transceiver
- UART Communication Speeds Up to 38,400 baud
- Integrated 3.3 V VDD LDO Regulator with Extended Peak Current Capability of 15 mA
- Supports Powering Slave Device from the Bus or from External Power Supply
- Adjustable I/O Levels
- Adjustable Constant Current Sink up to 2 or 6 Unit Loads Depending on the Package
- Low Bus Voltage Operation
- Extended Current Budget for External Circuits: at least 0.88 mA
- Polarity Independent
- Power-Fail Function
- Fast Startup – No External Transistor Required on STC Pin
- Industrial Ambient Temperature Range of -40°C to +85°C
- Available in:
 - ◆ 16-pin SOIC (Pin-to-Pin Compatible with TSS721A)
 - ◆ 20-pin QFN
- These are Pb-free Devices

Typical Applications

- Multi-energy Utility Meters
 - ◆ Water
 - ◆ Gas
 - ◆ Electricity
 - ◆ Heating systems

Related Standards – European Standard

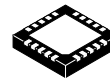
EN 13757-2, EN 1434-3

For more information visit www.m-bus.com

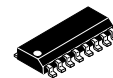


ON Semiconductor®

<http://onsemi.com>

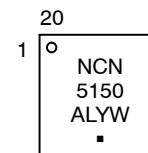


NQFP-20
MN SUFFIX
CASE 485E

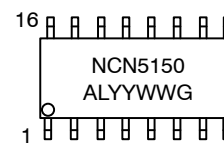


SOIC-16
D SUFFIX
CASE 751B

MARKING DIAGRAMS



NQFP-20



SOIC-16

A = Assembly Location
L = Wafer Lot (optional)
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NCN5150

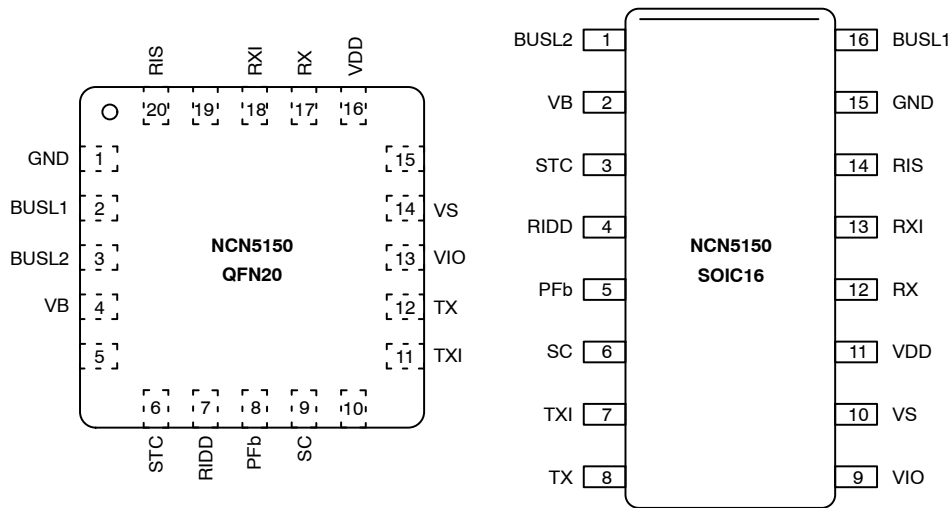


Figure 1. Pin Out NCN5150 in 20-pin NQFP and 16 Pin SOIC (Top View)

Table 1. NCN5150 PINOUT

| Signal Name | Type | Pin Number | | Pin Description |
|-------------|--------|--------------|---------------|--|
| | | NCN5150 SOIC | NCN5150 QFN | |
| BUSL1 | Bus | 16 | 2 | MBUS line. Connect to bus through 220 Ω series resistors. Connections are polarity independent |
| BUSL2 | Bus | 1 | 3 | |
| VB | Power | 2 | 4 | Rectified bus voltage |
| STC | Output | 3 | 6 | Storage capacitor pin. Connect to bulk storage capacitor (minimum 10 μ F, maximum 330 μ F–2,700 μ F – see Table 9) |
| RIDD | Input | 4 | 7 | Mark current adjustment pin. Connect to programming resistor |
| PFb | Output | 5 | 8 | Power Fail, active low |
| SC | Output | 6 | 9 | Mark bus voltage level storage capacitor pin. Connect to ceramic capacitor (typically 220 nF) |
| TXI | Output | 7 | 11 | UART Data output (inverted) |
| TX | Output | 8 | 12 | UART Data output |
| VIO | Input | 9 | 13 | I/O pins (RX, RXI, TX, TXI, PFb) high level voltage |
| VS | Output | 10 | 14 | Gate driver for PMOS switch between bus powered operation and external power supply |
| VDD | Power | 11 | 16 | Voltage regulator output. Connect to minimum 1 μ F decoupling capacitor |
| RX | Input | 12 | 17 | UART Data input |
| RXI | Input | 13 | 18 | UART Data input (inverted) |
| RIS | Input | 14 | 20 | Modulation current adjustment pin |
| GND | Ground | 15 | 1 | Ground |
| NC | NC | – | 5, 10, 15, 19 | Not connected pins. Tie to GND |
| EP | Ground | – | EP | Exposed Pad. Tie to GND |

NCN5150

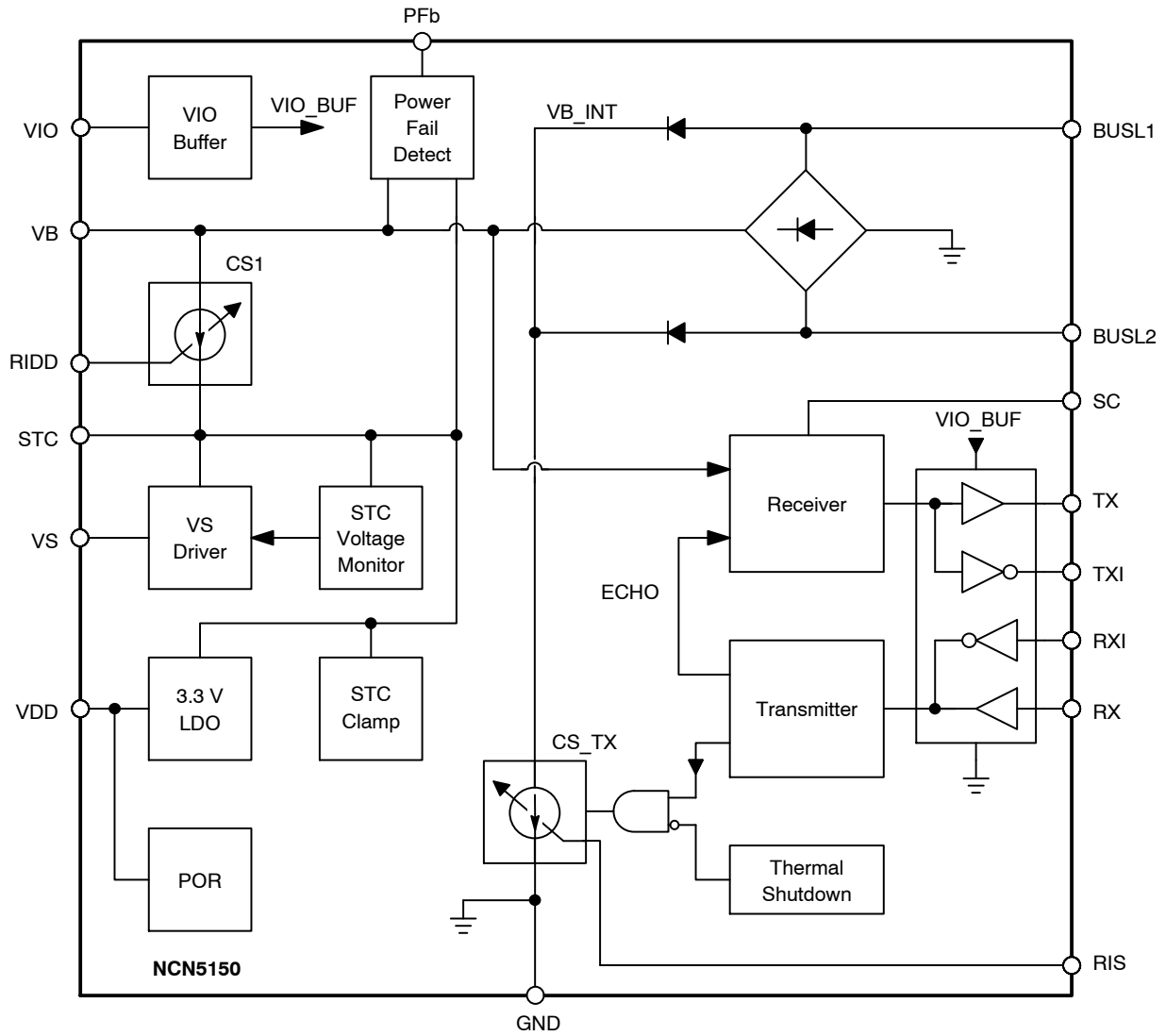


Figure 2. NCN5150 Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Min | Max | Unit |
|---------------------------|-----------------------------------|------|------|------|
| T_J | Junction Temperature | -40 | +150 | °C |
| T_S | Storage Temperature | -55 | +150 | °C |
| V_{BUS} | Bus Voltage (BUSL1 - BUSL2) | -50 | 50 | V |
| V_{TX}, V_{TXI} | Voltage on Pin TX, TXI | -0.3 | 7.5 | V |
| V_{RX}, V_{RXI}, V_{IO} | Voltage on Pin RX, RXI, VIO | -0.3 | 5.5 | V |
| ESD_{HBM} | ESD Rating - Human Body Model | 4.0 | - | kV |
| ESD_{MM} | ESD Rating - Machine Model | 250 | - | V |
| ESD_{CDM} | ESD Rating - Charged Device Model | 750 | - | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. All voltages are referenced to GND.

Table 3. THERMAL CHARACTERISTICS

| Rating | Symbol | Typical Value | Unit |
|--|-----------------|---------------|------|
| Thermal Characteristics, SOIC-16 – Thermal Resistance, Junction-to-Air | $R_{\theta JA}$ | 125 | °C/W |
| Thermal Characteristics, QFN-20 – Thermal Resistance, Junction-to-Air | $R_{\theta JA}$ | 42 | °C/W |

NOTE: $R_{\theta JA}$ obtained with 1S0P (SOIC) or 2S2P (QFN) test boards according to JEDEC JESD51 standard.

Table 4. RECOMMENDED OPERATING CONDITIONS (Notes 2 and 3)

| Symbol | Parameter | Min | Max | Unit | |
|-----------|---|----------------|-----|------|---|
| T_A | Ambient Temperature | -40 | +85 | °C | |
| V_{BUS} | Bus Voltage ($V_{BUSL1} - V_{BUSL2}$) | 1-2 Unit Loads | 9.2 | 42 | V |
| | | 3-6 Unit Loads | 9.7 | 42 | V |
| V_{IO} | VIO Pin Voltage (Note 4) | 2.5 | 3.8 | V | |

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

3. All voltages are referenced to GND.

4. V_{STC} must be at least 1V higher than V_{IO} for proper operation.

Table 5. ELECTRICAL CHARACTERISTICS (Note 5)

| Symbol | Parameter | Min | Typ | Max | Unit | |
|-------------------------|---|---|------|-----------------|------------|----|
| ΔV_{BR} | Voltage drop over bus rectifier ($V_{BUS} - V_B$) (R_{IDD} (Note 6) = 4.02 k Ω) | - | - | 1.25 | V | |
| ΔV_{CS} | Voltage drop over CS1 ($V_B - V_{STC}$) | R_{IDD} (Note 6) \geq 13 k Ω | 1.30 | - | - | V |
| | | R_{IDD} (Note 6) \leq 4.02 k Ω | 1.70 | - | - | |
| I_{BUS} | Total Current Drawn from the Bus, Mark State | R_{IDD} (Note 6) = 30 k Ω | - | 1.32 | 1.50 | mA |
| | | R_{IDD} (Note 6) = 13 k Ω | - | 2.71 | 3.00 | |
| | | R_{IDD} (Note 6) = 8.45 k Ω | - | 4.10 | 4.50 | |
| | | R_{IDD} (Note 6) = 6.19 k Ω | - | 5.50 | 6.00 | |
| | | R_{IDD} (Note 6) = 4.87 k Ω | - | 6.80 | 7.50 | |
| | | R_{IDD} (Note 6) = 4.02 k Ω | - | 8.22 | 9.00 | |
| ΔI_{BUS} | Bus Current Stability (over $\Delta V_{BUS} = 10$ V, RX/RXI = mark) | - | 0.2 | 2 | % | |
| I_{STC} | Idle Current Available for the Application to Draw from STC and V_{DD} (Including Current Drawn from IO Pins) | R_{IDD} (Note 6) = 30 k Ω | 0.88 | 1.05 | 1.20 | mA |
| | | R_{IDD} (Note 6) = 13 k Ω | 2.10 | 2.35 | 2.60 | |
| | | R_{IDD} (Note 6) = 8.45 k Ω | 3.10 | 3.60 | 4.00 | |
| | | R_{IDD} (Note 6) = 6.19 k Ω | 4.20 | 4.80 | 5.40 | |
| | | R_{IDD} (Note 6) = 4.87 k Ω | 5.30 | 6.10 | 6.90 | |
| | | R_{IDD} (Note 6) = 4.02 k Ω | 6.50 | 7.45 | 8.40 | |
| $\Delta I_{STC, space}$ | Additional Current Available for the Application when Transmitting a Space | - | 200 | - | μ A | |
| I_{CC} | Internal Supply Current (R_{IDD} (Note 6) = 13 k Ω , RX/RXI = mark) | - | 359 | 500 | μ A | |
| I_{IO} | Current Drawn by the V_{IO} Pin | -0.5 | - | 0.5 | μ A | |
| $V_{STC, clamp}$ | Clamp Voltage on Pin STC ($I_{DD} < I_{STC}$) | 6.0 | 6.5 | 7.0 | V | |
| V_B, PFb | Threshold Voltage on V_B to Trigger PFb (Note 7) | $V_{STC} + 0.3$ | - | $V_{STC} + 0.8$ | V | |
| $V_{PFb, OH}$ | PFb Voltage High ($I_{PFb} = -100$ μ A) | $V_{IO} - 0.6$ | - | V_{IO} | V | |
| $V_{PFb, OL}$ | PFb Voltage Low (Note 8) ($I_{PFb} = 50$ μ A) | 0 | - | 0.6 | V | |
| V_{RIDD} | Voltage on RIDD Pin | 1.15 | 1.20 | 1.25 | V | |
| $V_{VS, OH}$ | Voltage on VS during High State ($V_{STC} > V_{STC, VDD ON}$, $I_{VS} = -5$ μ A) | $V_{STC} - 0.4$ | - | V_{STC} | V | |
| $R_{VS, PD}$ | Pull-down Resistor on VS during Low State ($V_{DD} > 2$ V, $V_{STC} > V_S$) | 50 | 100 | 150 | k Ω | |

5. All voltages are referenced to GND.

6. Resistor with 1% accuracy.

7. PFb comparator has a 70 mV hysteresis.

8. PFb pin is pulled down with an on-chip resistor of typically 2 M Ω .

NCN5150

Table 6. VDD REGULATOR ELECTRICAL CHARACTERISTICS (Note 9)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------------|--|------|------|------|------|
| V _{DD} | Voltage on V _{DD} (Note 10) (I _{DD} < 15 mA) | 3.1 | 3.3 | 3.6 | V |
| I _{DD} | Peak Current that can be Supplied by V _{DD} (Note 11) | 15 | – | – | mA |
| I _{DD, OFF} | V _{BUS} = 0 V, V _{STC} = 0 V | –0.5 | – | 0.5 | μA |
| V _{POR, ON} | Power-on Reset Threshold, Release | 2.65 | 2.85 | 3.15 | V |
| V _{POR, OFF} | Power-on Reset Threshold, Reset | 2.55 | 2.75 | 3.00 | V |
| V _{STC, VDD ON} | Threshold Voltage on Pin STC to Turn On V _{DD} Regulator, Pull the VS Pin High and Enable the PF Function | 5.6 | 6.0 | 6.4 | V |
| V _{STC, VDD OFF} | Threshold Voltage on Pin STC to Turn Off V _{DD} Regulator and Pull the PFb and VS Pins Low | 3.7 | 4.0 | 4.3 | V |

9. All voltages are referenced to GND.

10. Including output resistance of V_{DD}.

11. Average current draw limited by I_{STC}.

Table 7. RECEIVER ELECTRICAL CHARACTERISTICS (Note 12)

| Symbol | Parameter | Min | Typ | Max | Unit | |
|-------------------------------|---|--|-----|----------------------------------|------|---|
| V _T | Receiver Threshold Voltage | V _{SC} – 8.2 | – | V _{SC} – 5.7 | V | |
| V _{SC} | Mark Level Storage Capacitor Voltage | – | – | V _B | V | |
| I _{SC, charge} | Mark Level Storage Capacitor Charge Current | –40 | –25 | –15 | μA | |
| I _{SC, discharge} | Mark Level Storage Capacitor Discharge Current | 0.3 | 0.6 | –0.033 × I _{SC, charge} | μA | |
| CDR | Charge/Discharge Current Ratio | 30 | 40 | – | | |
| V _{TX, OH, VTXI, OH} | TX/TXI High-level Voltage (I _{TX} /I _{TXI} = –100 μA) (Note 13) | V _{IO} – 0.6 | – | V _{IO} | V | |
| V _{TX, OL, VTXI, OL} | TX/TXI Low-level Voltage | (I _{TX} /I _{TXI} = 100 μA) | 0 | – | 0.35 | V |
| | | (I _{TX} = 1.1 mA) | 0 | – | 1.5 | V |
| I _{TX, ITXI} | V _{TX} = 7.5 V, V _{STC} = 6 V | 0 | – | 16 | μA | |

12. All voltages are referenced to GND.

13. V_{STC} must be at least 1 V higher than V_{IO} for proper operation.

Table 8. TRANSMITTER ELECTRICAL CHARACTERISTICS (Note 14)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------------|---|-----------------------|------|------|------|
| I _{MC} | Space Level Modulating Current (R _{RIS} = 100 Ω (Note 15)) | 12.5 | 15.0 | 18.0 | mA |
| V _{RIS} | Voltage on RIS Pin | 1.2 | 1.4 | 1.6 | V |
| V _{RX, IH, VRXI, IH} | RX/RXI Input High | V _{IO} – 0.8 | – | 5.5 | V |
| V _{RX, IL, VRXI, IL} | RX/RXI Input Low | 0 | – | 0.8 | V |
| I _{RX, IRXI} | Current Drawn or Sourced from RX/RXI Pins (Note 16) (V _{IO} = 3 V) | ±6 | – | ±30 | μA |

14. All voltages are referenced to GND.

15. Resistor with 1% accuracy.

16. Including internal pull-up resistor on RX and internal pull-down resistor on RXI.

NCN5150

APPLICATION SCHEMATICS

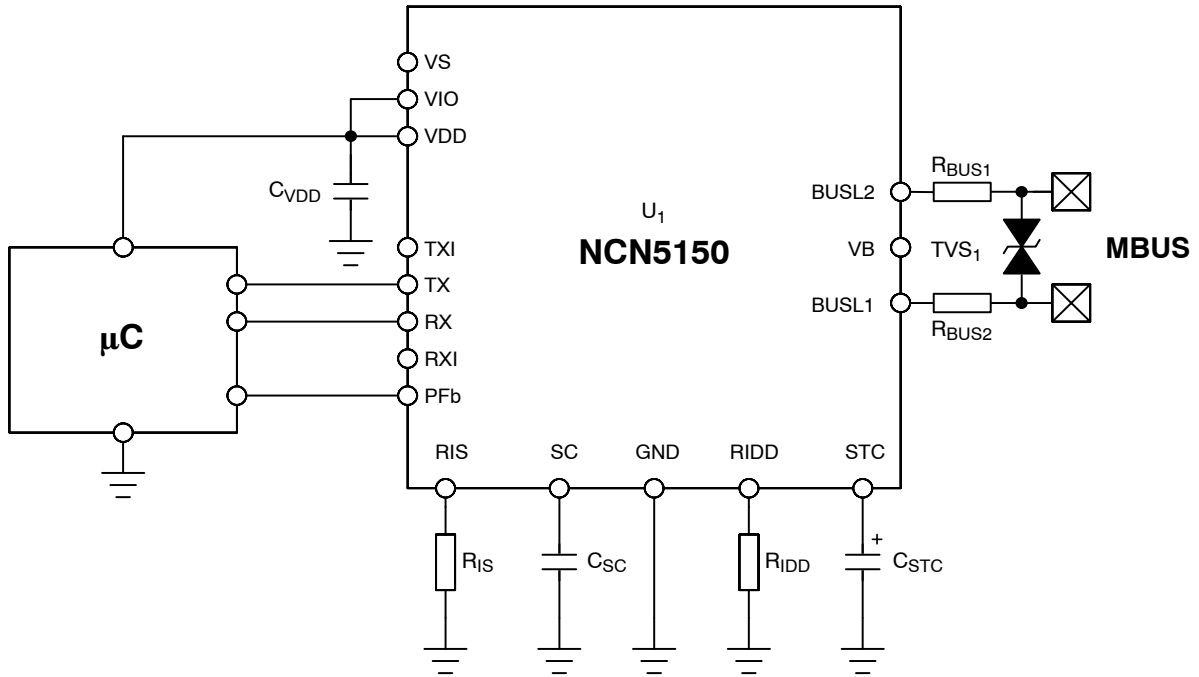


Figure 3. General Application Schematic

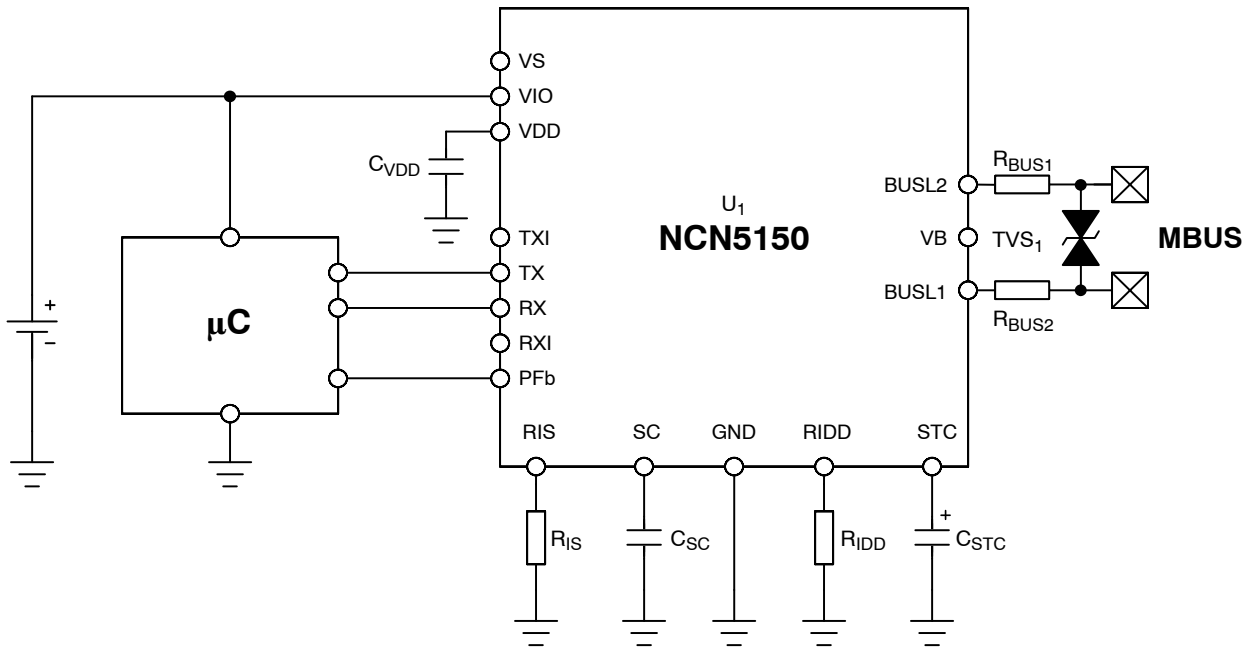


Figure 4. Application Schematic with External Power Supply (Battery)

NCN5150

APPLICATION SCHEMATICS

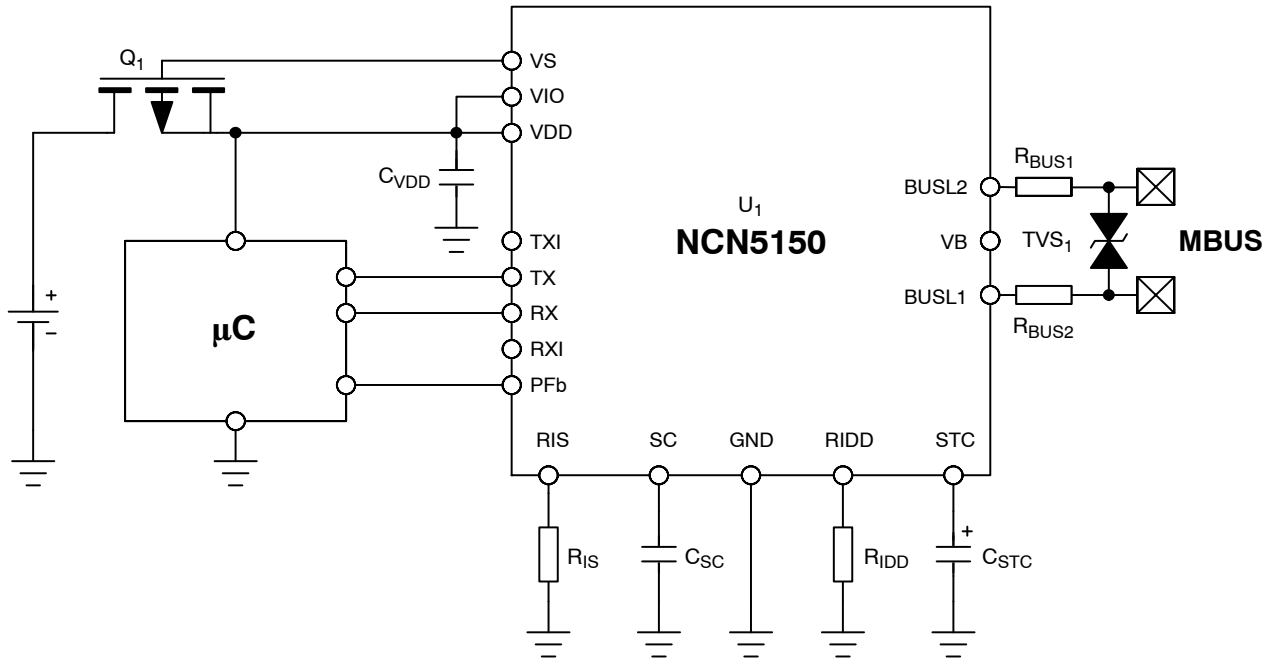


Figure 5. Application Schematic with Backup External Power Supply

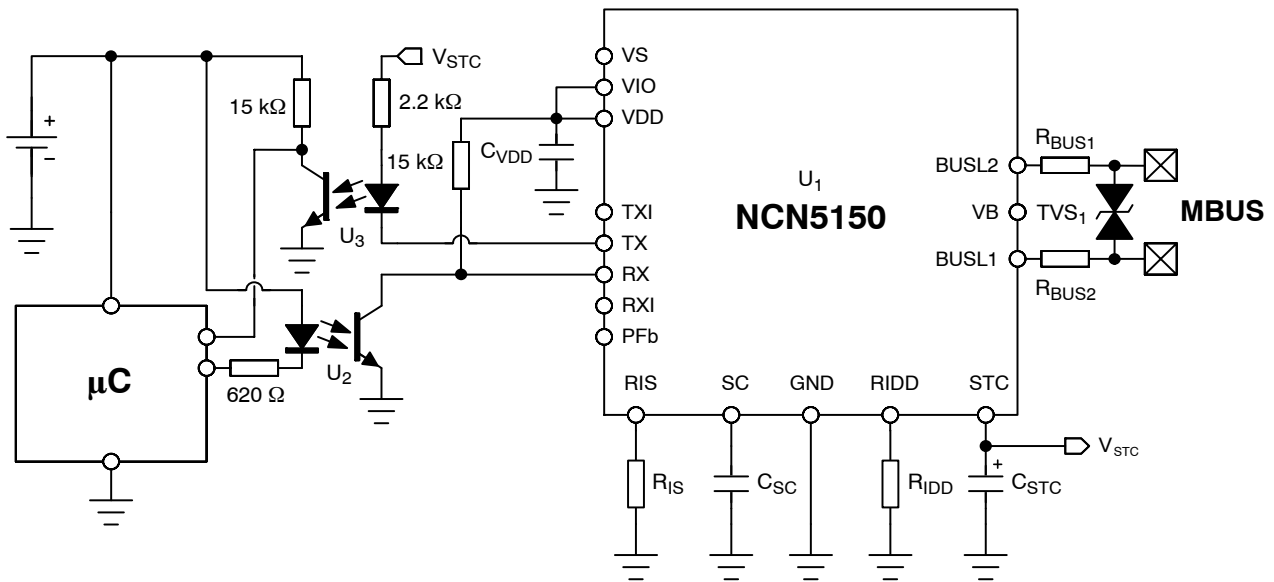


Figure 6. Optically Isolated Application Schematic

Table 9. TYPICAL BILL OF MATERIALS

| Reference Designator | Value (Typical) | Tolerance | Manufacturer | Part Number |
|---------------------------------------|-----------------|------------|------------------|-------------|
| U ₁ | – | – | ON Semiconductor | NCN5150 |
| TVS ₁ | 40 V | – | ON Semiconductor | 1SMA40CAT3G |
| C _{VDD} | > 1 μF | –20%, +80% | | |
| R _{IS} | 100 Ω | 1% | | |
| C _{SC} | 220 nF | –20%, +80% | | |
| R _{BUS1} , R _{BUS2} | 220 Ω | 10% | | |
| R _{IDD} | 1 UL | 30 kΩ | 1% | |
| | 2 UL | 13 kΩ | 1% | |
| | 3 UL | 8.45 kΩ | 1% | |
| | 4 UL | 6.19 kΩ | 1% | |
| | 5 UL | 4.87 kΩ | 1% | |
| | 6 UL | 4.02 kΩ | 1% | |
| C _{STC} | 1 UL | ≤ 330 μF | 10% | |
| | 2 UL | ≤ 820 μF | 10% | |
| | 3 UL | ≤ 1,200 μF | 10% | |
| | 4 UL | ≤ 1,500 μF | 10% | |
| | 5 UL | ≤ 2,200 μF | 10% | |
| | 6 UL | ≤ 2,700 μF | 10% | |

APPLICATION INFORMATION

The NCN5150 is a slave transceiver for use in the meter bus (M-BUS) protocol. The bus connection is fully polarity independent. The transceiver will translate the bus voltage modulation from master-to-slave communication to TTL UART communication, and in the other direction translate UART voltage levels to bus current modulation. The transceiver also integrates a voltage regulator for utilizing the current drawn in this way from the bus, and an early power fail warning. The transceiver also supports an external power supply and the I/O high level can be set to match the slave sensor circuit. A complete block diagram is shown in Figure 2. Each section will be explained in more detail below.

Meter Bus Protocol

M-BUS is a European standard for communication and powering of utility meters and other sensors. Communication from master to slave is achieved by voltage-level signaling. The master will apply a nominal +36 V to the bus in idle state, or when transmitting a logical 1 (“mark”). When transmitting a logical 0 (“space”), the master will drop the bus voltage to a nominal +24 V.

Communication from the slave to the master is achieved by current modulation. In idle mode or when transmitting a logical 1 (“mark”), the slave will draw a fixed current from the bus. When transmitting a logical 0 (“space”), the slave will draw an extra nominal 15 mA from the bus. M-BUS uses a half-duplex 11-bit UART frame format, with 1 start bit, 8 data bits, 1 even parity bit, and a stop bit.

Communication speeds allowed by the M-BUS standard are 300, 600, 2400, 4800, 9600, 19200 and 38400 baud, all of which are supported by the NCN5150.

Bus Connection and Rectification

The bus should be connected to the pins BUSL1 and BUSL2 through series resistors to limit the current drawn from the bus in case of failure (according to the M-BUS standard). Typically, two 220 Ω resistors are used for this purpose.

Since the M-BUS connection is polarity independent, the NCN5150 will first rectify the bus voltage through an active diode bridge.

Slave Power Supply (Bus Powered)

A slave device can be powered by the M-BUS or from an external supply. The M-BUS standard requires the slave to draw a fixed current from the bus. This is accomplished by the constant current source CS1. This current is used to charge the external storage capacitor C_{STC}. The current drawn from the bus is defined by the programming resistor R_{IDD}. The bus current can be chosen in increments of 1.5 mA called unit loads. Table 5 list the different values of programming resistors needed for different unit loads, as well as the current drawn from the bus (I_{BUS}) and the current that can be drawn from the STC pin (I_{STC}). I_{STC} is slightly less than I_{BUS} to account for the internal power consumption of the NCN5150. The R_{IDD} resistor used must be at least 1%

accurate. Note that using 5 and 6 Unit Loads is not covered by the M-BUS standard.

When the voltage on the STC pin reaches V_{STC} , VDD ON the LDO is turned on, and will regulate the voltage on the VDD pin to 3.3 V, drawing current from the storage capacitor. A decoupling capacitor of minimum 1 μ F is required on the VDD pin for stability of the regulator. On the STC pin, a minimum capacitance of 10 μ F is required. Furthermore, the ratio C_{STC}/C_{VDD} must be larger than 9. The voltage on the STC pin is clamped to $V_{STC, clamp}$ by a shunt regulator, which will dissipate any excess current that is not used by the NCN5150 or external circuits.

Slave Power Supply (External)

In case the external sensor circuit consumes more than the allowed bus current or the sensor should be kept operational when the bus is not present, an external power supply, such as a battery, is required.

When the external circuitry uses different logical voltage levels, simply connect the power supply of that voltage level to V_{IO} , so that the RX, RXI, TX, TXI and Pfb pins will respond to the correct voltage levels. The NCN5150 will still be powered from the bus, but all communication will be translated to the voltage level of V_{IO} .

If the external power supply should be used only as a backup when the bus power supply fails, a PMOS transistor can be inserted between the external power supply and VDD as shown in Figure 5. The gate is connected to VS, and will be driven high when the voltage on STC goes above the turn-on threshold of the LDO, nl. $V_{STC, VDD ON}$. For more information see the paragraph on the power on sequence and corresponding Figure 12 on page 10.

Communication, Master to Slave

M-BUS communication from master to slave is based on voltage level signaling. To differentiate between master signaling and voltage drop caused by the signaling of another slave over cabling resistance, etc., the mark level $V_{BUS, MARK}$ is stored, and only when the bus voltage drops to less than V_T will the NCN5150 detect communication. A simplified schematic of the receiver is shown in Figure 8. The received data is transmitted on the pins TX and TXI, as shown in the waveforms of Figure 7.

An external capacitor must be connected to the SC pin to store the mark voltage level. This capacitor is charged to V_B . Discharging of this capacitor is typically 40x slower, so that the voltage on SC drops only a little during the time the master is transmitting a space. The value of C_{SC} must be chosen in the range of 100 nF–330 nF.

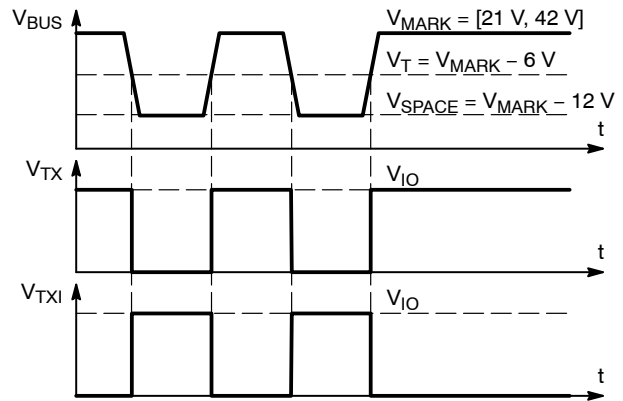


Figure 7. Communication, Master to Slave

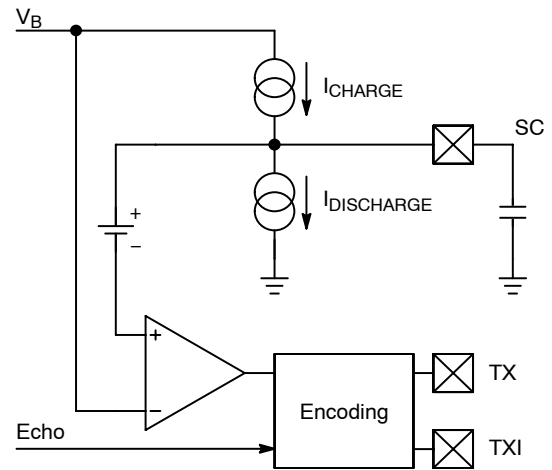


Figure 8. Communication, Master to Slave

Communication, Slave to Master

M-BUS communication from slave to master uses bus current modulation while the voltage remains constant. This current modulation can be controlled from either the RX or RXI pin as shown in Figure 10. When transmitting a space (“0”), the current modulator will draw an additional current from the bus. This current can be set with a programming resistor R_{RIS} . To achieve the space current required the M-BUS standard, R_{RIS} should be 100 Ω . A simplified schematic of the transmitter is shown in Figure 11.

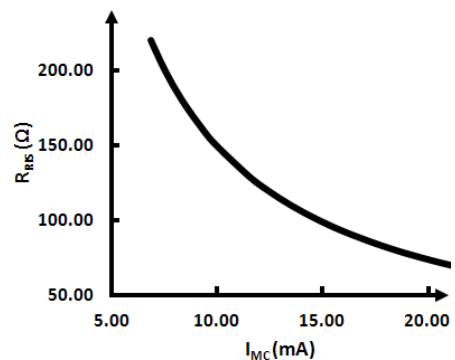


Figure 9. Typical Relationship between RIS and Current Modulation Level

NCN5150

Because the M-BUS protocol is specified as half-duplex, an echo function will cause the transmitted signal on RX or RXI to appear on the receiver outputs TX and TXI. Should the master attempt to send at the same time, the bitwise added signal of both sources will appear on these pins, resulting in invalid data.

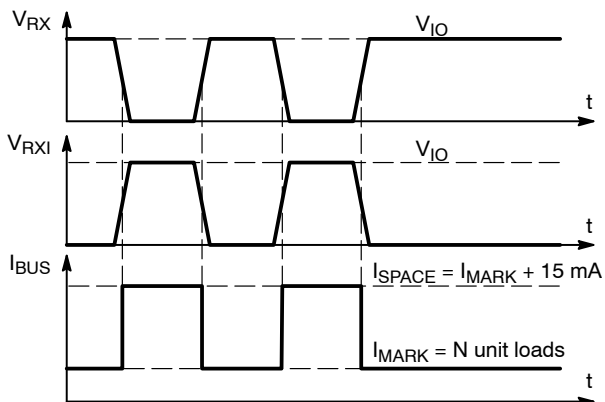


Figure 10. Communication, Slave to Master

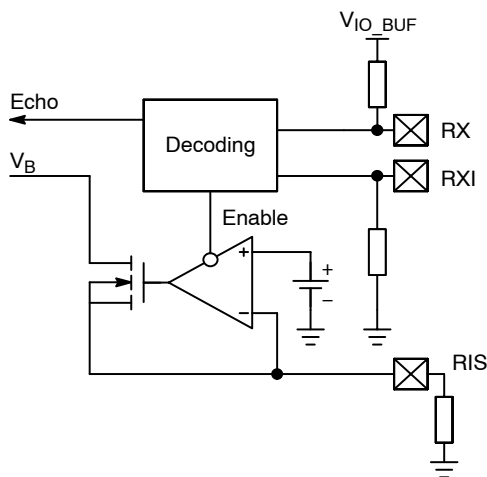


Figure 11. Communication, Slave to Master

Power On/Off Sequence

The power-on and power-off sequence of the NCN5150 is shown in Figure 12. Shown also in Figure 12 is the operation of the PFB pin. This pin is used to give an early warning to the microcontroller that the bus power is collapsing, allowing the microcontroller to save its data and

shut down gracefully. The times t_{on} and t_{off} can be approximated by the following formulas:

$$t_{on} = \frac{C_{STC}}{I_{STC}} V_{STC, VDD ON} \quad (\text{eq. 1})$$

$$t_{off} = \frac{C_{STC}}{I_{CC} + I_{DD}} (V_{STC, Clamp} - V_{STC, VDD OFF}) \quad (\text{eq. 2})$$

Where I_{CC} is the internal current consumption of the NCN5150 and I_{DD} is the current consumed by external circuits drawn from either VDD or STC.

These formulas can be used to dimension the value of the bulk C_{STC} needed, taking into account that the M-BUS standard requires t_{on} to be less than 3 s.

For certain applications where the power drawn from the bus is not used in external circuits, the storage capacitor value can be much lower. The NCN5150 requires a minimum STC capacitance of 10 μF to ensure that the bus current regulation is stable under all conditions.

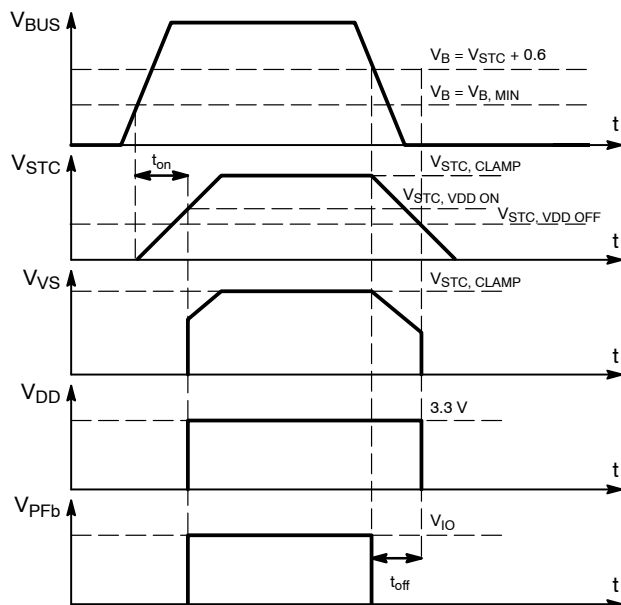


Figure 12. Power-on and Power-off

Thermal Shutdown

The NCN5150 includes a thermal shutdown function that will disable the transmitter when the junction temperature of the IC becomes too hot. The thermal protection is only active when the slave is transmitting a space to the master.

Table 10. ORDERING INFORMATION

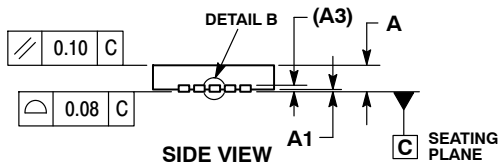
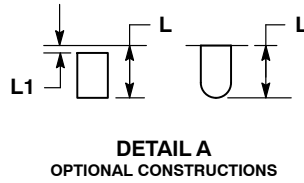
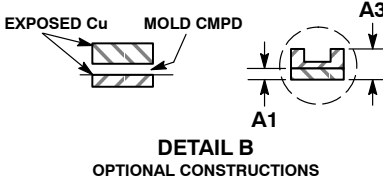
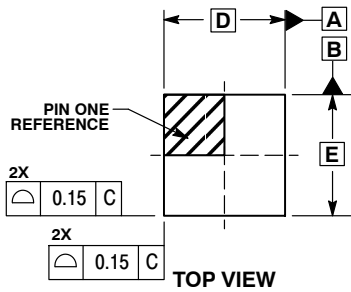
| Device | Package | Shipping [†] |
|--------------|--------------------------|-----------------------|
| NCN5150DG | SOIC16 (Pb-free) | 48 Units / Tube |
| NCN5150DR2G | | 3,000 / Tape & Reel |
| NCN5150MNTWG | NQFP20, 4x4 (Pb-free) | 2,500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCN5150

PACKAGE DIMENSIONS

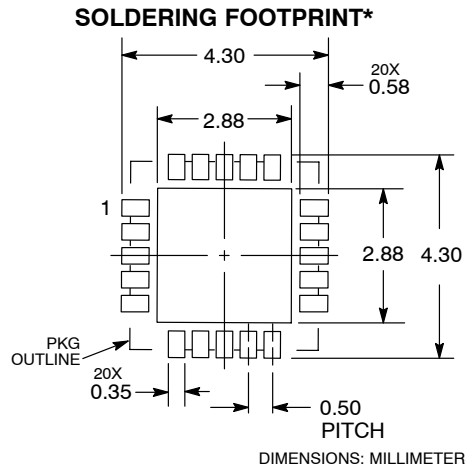
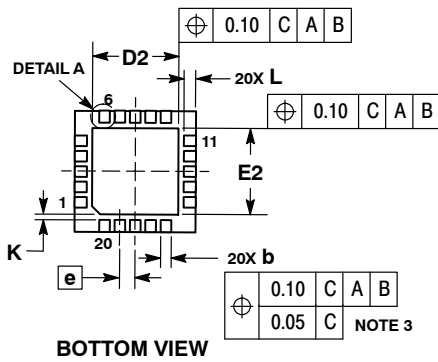
QFN20, 4x4, 0.5P
CASE 485E
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 4.00 BSC | |
| D2 | 2.60 | 2.90 |
| E | 4.00 BSC | |
| E2 | 2.60 | 2.90 |
| e | 0.50 BSC | |
| K | 0.20 REF | |
| L | 0.35 | 0.45 |
| L1 | 0.00 | 0.15 |

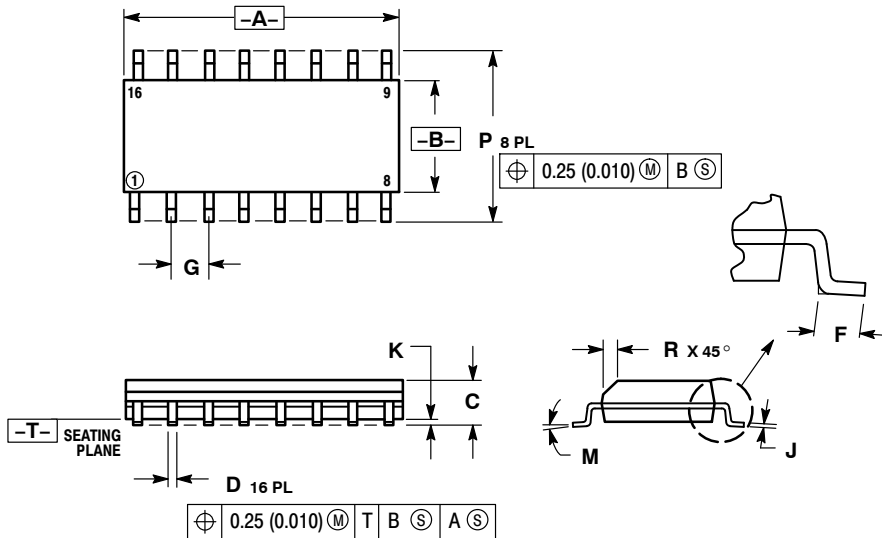


*For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCN5150

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

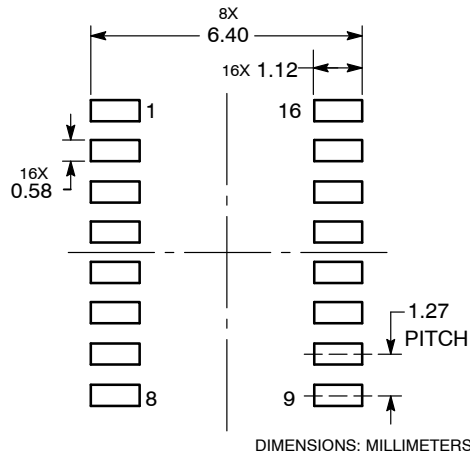


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative